

ABSTRACT OF THE DISCLOSURE

Disclosed is an improved liquid crystal display to minimize delays of data signals and control signals on source PCB and the EMI. The liquid crystal display includes a wire aggregation that is arranged on a source PCB. The wire aggregation transmits signals including data signals, control signals, and clock signals of which frequency is lowered to a half. The wire aggregation is symmetrically separated into a first group of wires for transmitting a first image signal and a second group of wires for transmitting a second image signal. The first group of wires are connected to one side of corresponding source drive integrated circuits and the second group of wires are connected to the other side of corresponding source drive integrated circuits.

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